

TSMC-99-274B



May 3, 2002

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To: Commissioner of Patents and Trademarks  
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Fr: George O. Saile, Reg. No. 19,572  
20 McIntosh Drive  
Poughkeepsie, N.Y. 12603

Subject:

Serial No. 10/084,082 02/27/02

Kong-Beng Thei, Ming-Dar Lei,  
Shou-Gwo Wu

SALICIDE FIELD EFFECT TRANSISTORS  
WITH IMPROVED BORDERLESS CONTACT  
STRUCTURES AND A METHOD OF  
FABRICATION

Grp. Art Unit: 2812

#### INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation  
In An Application.

The following Patents and/or Publications are submitted to  
comply with the duty of disclosure under CFR 1.97-1.99 and  
37 CFR 1.56. Copies of each document is included herewith.

#### CERTIFICATE OF MAILING

I hereby certify that this correspondence is being  
deposited with the United States Postal Service as first class  
mail in an envelope addressed to: Commissioner of Patents and  
Trademarks, Washington, D.C. 20231, on May 14, 2002.

Stephen B. Ackerman, Reg.# 37761

Signature/Date

*Stephen B. Ackerman* 5/14/02

U.S. Patent 5,858,846 to Tsai et al., "Salicide Integration Method", discloses a method for making salicide FETs in which arsenic ions are implanted in a titanium (Ti) metal layer prior to annealing to inhibit Si diffusion in Ti and eliminate bridging between the source/drain and gate electrode.

U.S. Patent 5,744,395 to Shue et al., "Low Resistance, Self-Aligned, Titanium Silicide Structures, Using a Single Rapid Thermal Anneal Procedure", discloses a method where a Ti layer is deposited at an elevated temperature to form a silicide which is removed in a wet etch and then requires only a single RTA.

U.S. Patent 5,702,972 to Tsai et al., "Method of Fabricating MOSFET Devices", discloses a double spacer method in which the second spacer is removed after the silicide is formed.

U.S. Patent 5,899,742 to Sun, "Manufacturing Method for Self-Aligned Local Interconnects and Contacts Simultaneously", describes a method for making aligned local inter-connections and contacts simultaneously to FETs.

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U.S. Patent 5,840,624 to Jang et al., "Reduction of Via Over Etching for Borderless Contacts", describes a method for etching borderless contacts on multilevel metal layers without overetching.

Sincerely,

A handwritten signature in black ink, appearing to read 'SBA', is written over the typed name.

Stephen B. Ackerman,  
Reg. No. 37761